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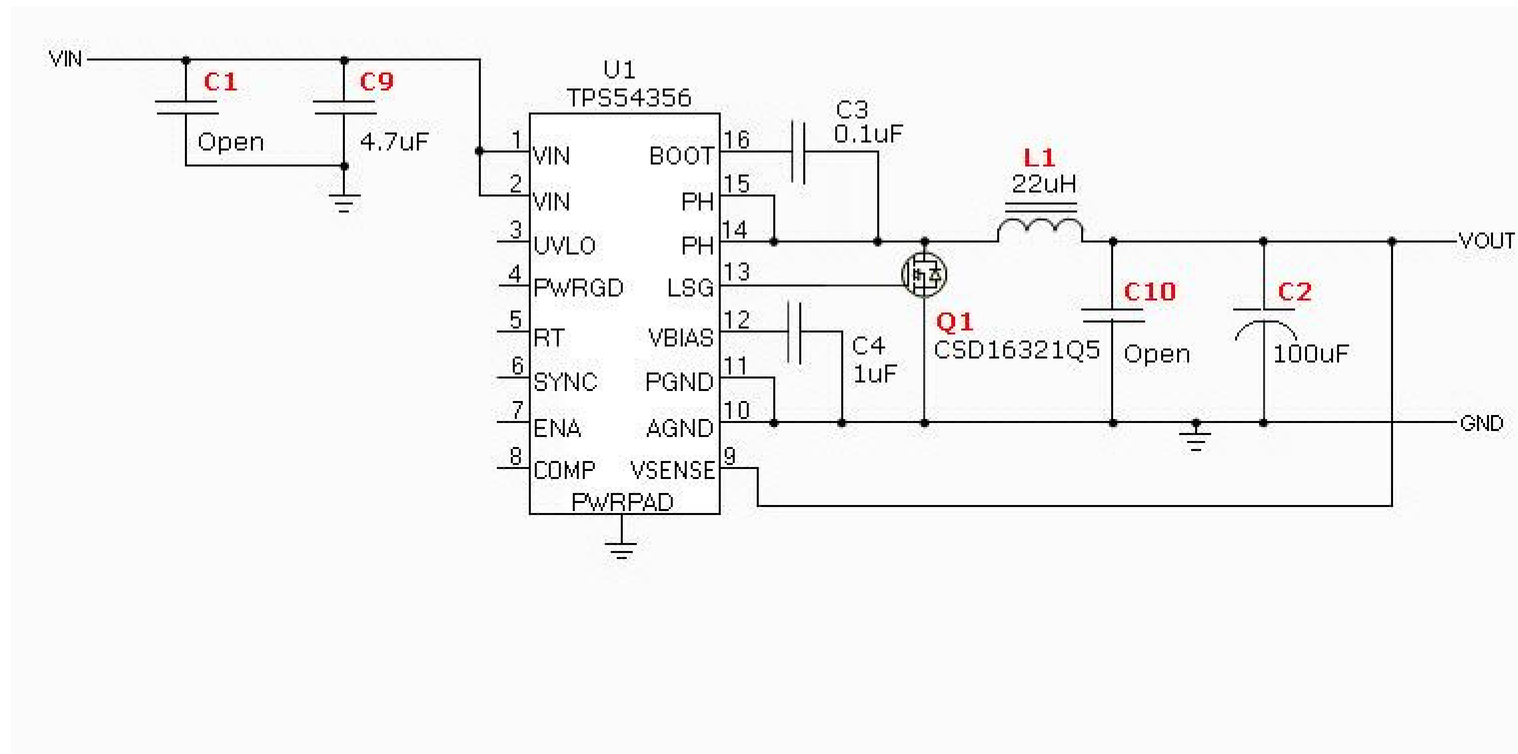
Design Summary

Design Name: **TPS54356 18-6V to 3.3V @ 3A. 04/09/2010 13:38:26**

Design ID:	**101428**	Created By User:	**Emanuel Avila**
Creation Date:	**09 Apr 2010**	Design Type:	**PowerSupply**
Local Time:	**01:38 PM**		

Schematic



Analysis

Analysis - Main

Parameter	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum	Units
Input Voltage	6.00	-	18.00	-	-	-	-	-	-	Volts
Input Ripple	-	-	-	-	-	360	-	-	415	mVp-p
UVLO(Start)	-	-	-	-	-	-	-	-	-	Volts
UVLO(Stop)	-	-	-	-	-	-	-	-	-	Volts
Switching Frequency	-	-	-	-	500	-	-	-	-	KHz
Slow Start	-	-	-	-	4	-	-	-	-	ms
Estimated PCB Area	-	-	-	-	-	-	-	825	-	mm²
Max Component Height	-	-	-	-	-	25	-	-	7	mm

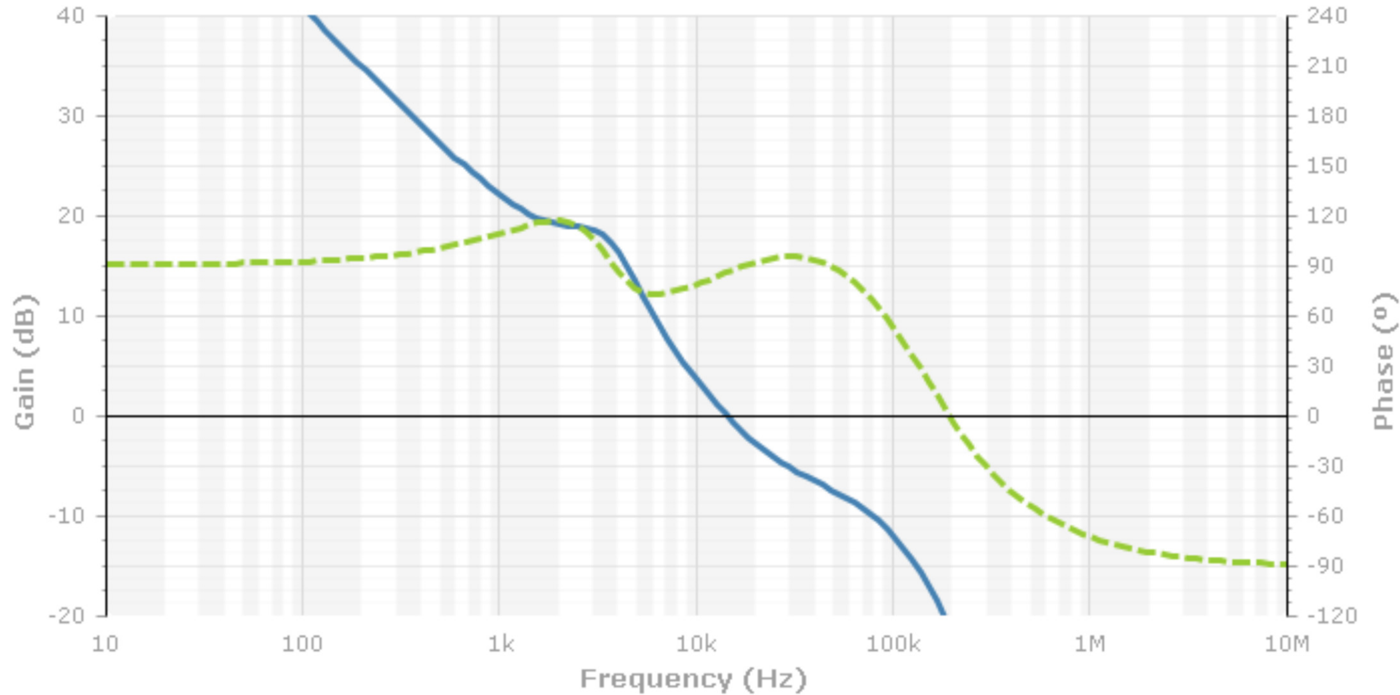
Analysis - Output1

Parameter	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum	Units
Output Voltage	-	3.300	-	-	-	-	3.291	-	3.309	Volts
Output Ripple	-	-	-	-	-	66	-	-	19	mVp-p
Output Current	-	-	3.000	0.100	-	-	-	-	-	Amps
Inductor Peak to Peak Current	-	-	-	-	-	-	0.181	-	0.321	Amps
Current Limit Threshold	-	-	-	-	4.5	-	-	-	-	Amps
Gain Margin	-	-	-	-10	-	-	-	-21	-	dB
Phase Margin	-	-	-	60	-	-	-	86	-	Deg.
Upper FET RDSon	-	-	-	-	-	-	121	-	152	mOhms
Lower FET RDSon	-	-	-	-	-	-	2	-	2	mOhms
Duty Cycle	-	-	-	-	-	-	19.4	-	61.7	%
On Time Min(switch)	-	-	-	-	-	-	323.5	-	1542.1	ns
Cross Over Frequency	-	-	-	-	-	-	-	14	-	KHz

Loop Response

LoopResponse - Output1

Switching Freq	Cross Over Freq	LC Corner Freq	ESR Zero Freq	Gain Margin	Phase Margin
500Khz	**14.4Khz**	**3.4Khz**	**26.5Khz**	**-21 dB**	**86 Deg.**



Scale Up

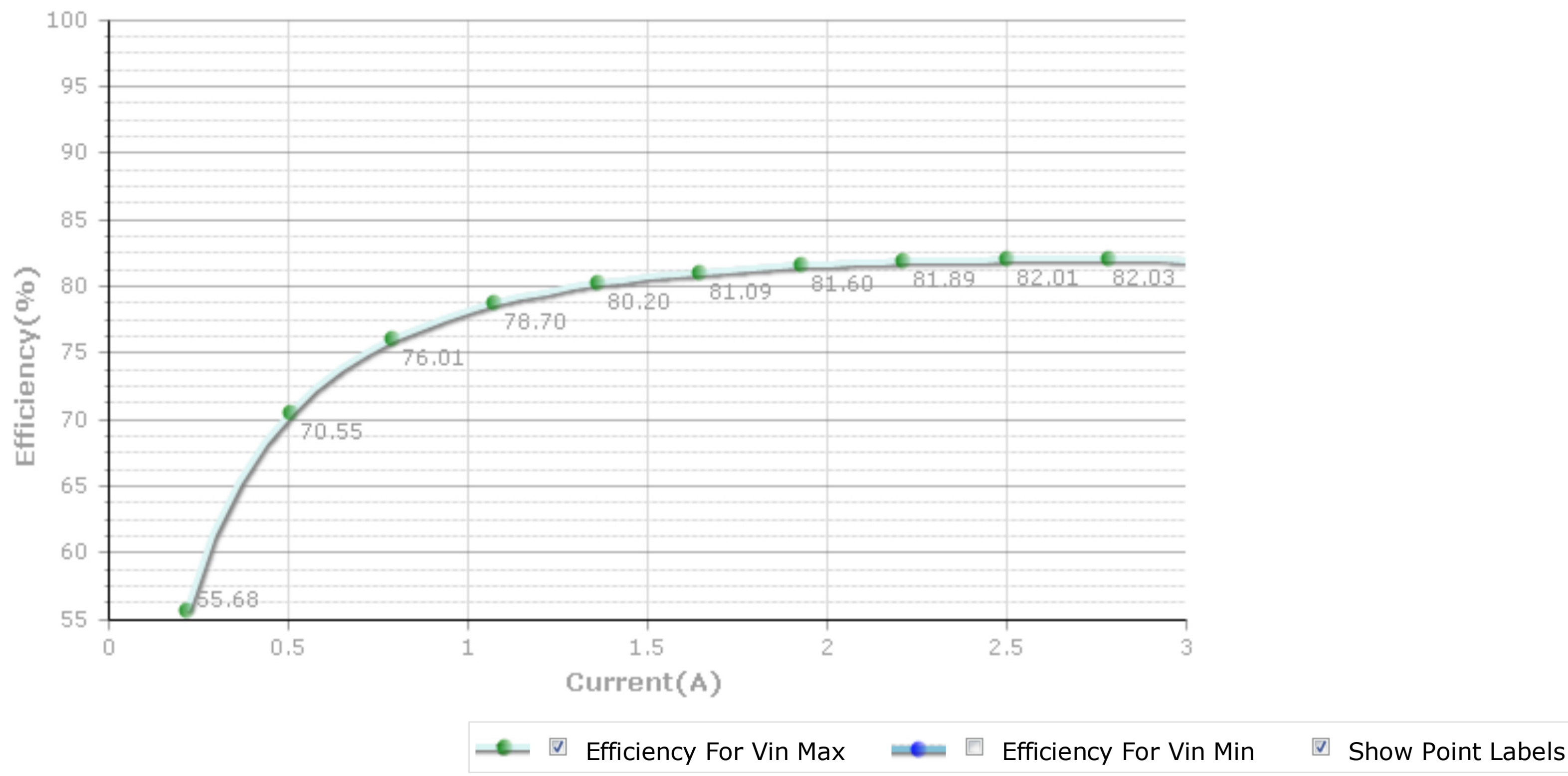
Scale Down

This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Maximum Load, and Maximum Capacitor ESR. To customize conditions use the "What If Analysis" form

- ☐ Open Loop Error Amplifier Gain
- ☐ Compensated Error Amplifier Gain
- ☐ Compensated Error Amplifier Phase
- ☐ Power Stage Gain
- ☐ Power Stage Phase
- ☑ Total Gain
- ☑ Total Phase

Efficiency

Efficiency - Output1



Stress

Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	25V	18.1V	2.5A	1.5A		11mW	-
C2 (Bulk Output Cap)	16V	3.32V	2.55A	93mA		517uW	-
L1 (Output Inductor)	-	-	4A	3A		355mW	-
Q1 (Sync. Rectifier)	25V	18.1V	100A	2.69A		141mW	30˚C
U1 (Converter)	21V	18.1V	6.5A	2.36A		1.7W	95˚C

Each loss in this view is the worst case calculation for the individual component. The conditions that cause the worst case loss will not all occur at the same time for all components. Therefore adding up the individual worst cases losses to get a total loss of the system is not realistic.

Max Junction Temperature is calculated using Ambient Temperature 25°C along with the resistance (junction to ambient) specified by the manufacturer, with their standards for board layout.

It is recommended that the user review the specifications given by the FET manufacturer for their board layout standards.

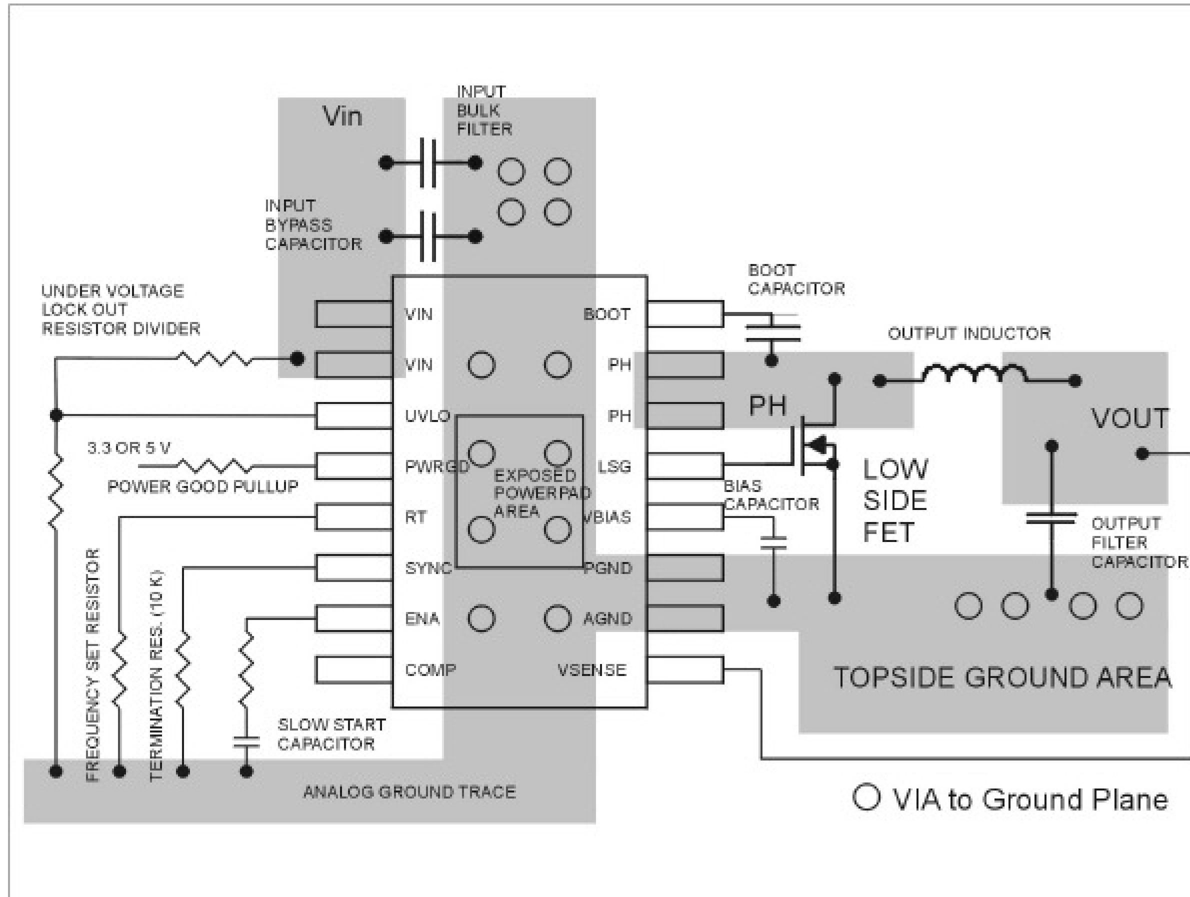
Using a low cost PCB with minimal copper will have a great impact on heat dissapation and could lead to much higher junction temperatures.

Calculated Voltage does not take into account spike voltages caused by various parasitic inductances and capacitances that are factors of board layout

Bill Of Materials

Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C2	1	TPSD107M016R0060	Capacitor, NA, 100uF, 16V, 20%	AVX	7343-31	30	3
C3	1	Standard	Capacitor, Ceramic, 0.1uF, 20V, 1%	Standard	0805	3	1
C4	1	Standard	Capacitor, Ceramic, 1uF, 20V, 1%	Standard	0805	3	1
C9	1	GRM21BR61E475KA12L	Capacitor, Ceramic, 4.7uF, 25V, 10%	muRata	GRM21B 0805	3	1
L1	1	744 571 22	Inductor, 22uH, 4A, 39.4mΩ	Wurth Elektronik eiSos	774571	330	7
Q1	1	CSD16321Q5	Transistor, NFET, 25V, 100A, 3mΩ	Texas Instruments, Inc.	QFN 5x6	31	1
R15	1	Standard	Resistor, SurfaceMount, 0.0Ω, 0W, 1%	Standard	0805	3	1
R7	1	Standard	Resistor, SurfaceMount, 0.0Ω, 0W, 1%	Standard	0805	3	1
U1	1	TPS54356	IC, Converter, 16 pins	Texas Instruments, Inc.	HTSSOP-Power PAD	34	2

Layout



Layout Guidelines:

TPS5435x

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS54350 ground pins. The minimum recommended bypass capacitance is 10-μF ceramic with a X5R or X7R dielectric and the optimum placement is closest to the VIN pins and the AGND and PGND pins. See Figure 21 for an example of a board layout. The AGND and PGND pins should be tied to the PCB ground plane at the pins of the IC. The source of the low-side MOSFET and the anode of the Schottky diode should be connected directly to the PCB ground plane. The PH pins should be tied together and routed to the drain of the low-side MOSFET or to the cathode of the external Schottky diode. Since the PH connection is the switching node, the MOSFET (or diode) should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The recommended conductor width from pins 14 and 15 is 0.050 inch to 0.075 inch of 1-ounce copper. The length of the copper land pattern should be no more than 0.2 inch.

For operation at full rated load, the analog ground plane must provide adequate heat dissipating area. A 3-inch by 3-inch plane of copper is recommended, though not mandatory, dependent on ambient temperature and airflow. Most applications have larger areas of internal ground plane available, and the PowerPAD should be connected to the largest area available. Additional areas on the bottom or top layers also help dissipate heat, and any area available should be used when 3 A or greater operation is desired. Connection from the exposed area of the PowerPAD to the analog ground plane layer should be made using 0.013-inch diameter vias to avoid solder wicking through the vias. Four vias should be in the PowerPAD area with four additional vias outside the pad area and underneath the package. Additional vias beyond those recommended to enhance thermal performance should be included in areas not under the device package.